113072

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Date 1/29/04 Serial # 10/002,447 Priority Application Date _____

Your Name M. Lewis Examiner # 73172

AU 2822 Phone 272-1835 Room 5A30

In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

01-29-04 P03:46 IN

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____

Secondary Refs ✓ Foreign Patents ___ _____

Teaching Refs ___ _____

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-9

Problem: See Pages 1+2

Solution: " " 2+3

Staff Use Only	Type of Search	Vendors
Searcher: HERRERA	Structure (#)	STN ✓
Searcher Phone: 272-2663	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, ~~CP4-9C18~~ JEF 4B68	Litigation	Questel/Orbit
Date Searcher Picked Up: 2/4/04	Fulltext	Lexis-Nexis
Date Completed: 2/5/05	Patent Family	WWW/Internet
Searcher Prep/Rev Time: 360	Other	Other
Online Time: 65		

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     FILE 'HCAPLUS, WPIX' ENTERED AT 15:25:04 ON 04 FEB 2004
L1             2 S US2003080393/PN
L2               SEL PLU=ON  L1 1- MC IC :      8 TERMS
L3         79141 S L2
L4         97216 S L3 OR (H01L027-02 OR H01L027-34 OR H01L023-48)/IC
L5       1257211 S FUSE# OR FUS!BL? OR BLOW!BL? OR LINK? OR OR VOLATIL?
L6       1821841 S CONDUCT?(2A)(POLYMN OR POLYMER#) OR ORGANIC# OR POLYIMIDE# OR
                  POLYAMIDE# OR POLYARYLENE#(2A) ETHER# OR POLYAROMATIC#(2A) HYDRO
                  CARBON# OR PAH OR POLYANILINE# OR SILK OR FLARE OR VELOX OR
                  ORMECON OR DLC OR DIAMOND(2A) CARBON
L7          1399 S L5 AND L6 AND L4
L8       4371439 S PHOTOCAT? OR (PHOTO OR LIGHT OR PHOTOLY?
                  OR ULTRAVIOLET? OR ULTRA(W)VIOLET? OR UV# OR SUV OR LUV OR
                  RADIA? OR IRRADIA? OR EMANAT? OR EMIT? OR EMISS? OR LASER?)
L9             2 S L7 AND L8
L10          455 DUP IDENTIFY L9 (INCLUDES 1 SET OF DUPLICATES)
L11            1 S L10 NOT P/DT
L12          454 S L10 NOT L11
L13       250877 S FUSE OR FUSES OR FUSED OR FUS!BL? OR
                  BLOW!BL? OR VOLATILIZ?
L14           84 S L13 AND L4 AND L6 AND L8
L15         9773 S L13(5A)(L8 OR SEMICONDUCT? OR IC OR
                  INTEGRATED CIRCUIT#)
L16           20 S L15 AND L14
L17      1761333 S CONDUCT?(2A) POLYMER# OR ORGANIC# OR
                  POLYIMIDE# OR POLYAMIDE# OR POLYARYLENE#(2A) ETHER# OR
                  POLYAROMATIC#(2A) HYDROCARBON# OR PAH OR POLYANILINE#
L18       147277 S FUSE OR FUSES OR (FUSE!BLE? OR FUS!BL?)(2A)
                   LINK? OR VOLATILIZ? OR VOLATILIS? OR BLOW!BL? OR CIRCUIT?(2A)
                  BREAK? OR ANTIFUSE? OR SWITCH!BLE?
L19      1239130 S SEMICONDUCT? OR IC OR INTEGRATED CIRCUIT#
L20         4183 S L18(5A) L19
L21          108 S L17 AND L20
L22           94 S L21 NOT L16
L23           90 S L22 AND P/DT
L24           31 S L23 AND (US OR WO)/PRC
L25           28 S L24 NOT PRD>20011026
L26           50 S L22 NOT L24 NOT PD>20011026
L27           50 S L26 NOT PY>2001
L28           78 S L25 OR L27
L29      2661230 S LINER# OR LINING# OR WRAP? OR BINDING? OR
                  COAT?
L30           24 S L28 AND L29
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DIALOG(R)File  34:SciSearch(R) Cited Ref Sci
(c) 2004 Inst for Sci Info. All rts. reserv.

S1       4  CA='SRIKRISHNAN KV'

File 342:Derwent Patents Citation Indx  1978-04/200402
       (c) 2004 Thomson Derwent
S1       1  PN='US 5469981'
MAP PN T/CT=
S3       4  CT=US 5469981
map anpr


File 350:Derwent WPIX  1963-2004/UD,UM &UP=200408
       (c) 2004  Thomson Derwent
S1      10  AN=DE 19738575 + AN=TW 99120812 + AN=US 52018 + AN=US 541488
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1/a/5

DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.
012850321 **Image available**
WPI Acc No: 2000-022153/200002
Transient pulse current tolerable thin type fuse for electrical devices
Patent Assignee: UCHIHASHI ESTEC KK (UCHI-N)
Inventor: KAWANISHI T
US 5982268 A 19991109 US 9852018 A 19980331 200002 B
Priority Applications (No Type Date): US 9852018 A 19980331
Abstract (Basic): US 5982268 A

NOVELTY - Thin type fuse consists of plastic insulating substrate film (1) and a pair of band-like lead conductors (2) each having emerging portion (210) at the tip portion. A fuse element (3) is connected in-between the emerging portions (210) by welding or brazing. A **plastic insulating covering film** (4) which is in direct contact with fuse element forms the outermost layer of the fuse.

DETAILED DESCRIPTION - Flux is filled in the space between insulating substrate film (1) and insulating covering film (4) and both are made up of the same materials like polyethylene terephthalate, polyamide etc. **Insulative film forms the substrate for fuse element.**

USE - To protect electrical devices against transient pulse overcurrent flow.

ADVANTAGE - Thin type fuse reduces the mounting space because of smaller size. Keeps the initial fusing characteristics without changing even when transient pulse overcurrent flow is repeated.

Derwent Class: X13
International Patent Class (Main): H01H-085/046
International Patent Class (Additional): H01H-069/02; H01H-085/044
Manual Codes (EPI/S-X): X13-D01A; X13-D01T5

L9 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:502474 HCAPLUS
TI Self-aligned **fuse** structure with increased density and reduced thermal exposure and method of fabrication with heat sink
IN Giust, Gary K.; Castagnetti, Ruggero; Liu, Yauh-ching; Ramesh, Subramanian
PA Lsi Logic Corporation, USA
PI US 6259146 B1 20010710 US 1998-118232 19980717
PRAI US 1998-118232 19980717
AB Provided are a self-aligned semiconductor **fuse** structure, a method of making such a **fuse** structure, and apparatuses incorporating such a **fuse** structure. The **fuse** break point, that point at which the elec. **link** of which the **fuse** is part is severed by a **laser** beam, is self-aligned using photolithog. patterned dielec. and a heat sink material. The self-alignment allows the size and location of the break point to be more forgiving of the **laser** beam size and alignment. This has several advantages, including allowing photolithog. control and effective size reduction of the **laser** spot irradiating the **fuse** material and surrounding structure. This permits reduced **fuse** pitch, increasing d. and the efficiency of use of chip area, and results in reduced thermal exposure, which causes less damage to chip. In addition, **laser** alignment is less critical and therefore less time-consuming, which increases throughput in fabrication. The present invention exploits the characteristic of most dielec. materials that they are poor conductors of thermal energy. Thermal resistance increases with the thickness of the dielec. Thus that heat is conducted more easily and thus quickly through a relatively thin portion of dielec. than it is through a relatively thick portion of dielec. In alternative embodiments, the present invention also exploits the characteristic of a dielec. material that its reflectance changes with its thickness due to optical interference effects. In such embodiments, the self-alignment of the **fuse** break point is further facilitated using photolithog. and anti-reflective coatings.
IC ICM **H01L029-00**
ICS H01L027-10
NCL 257529000
ST **fuse laser** photolithog heat sink
IT Memory devices
(DRAM (dynamic random access); self-aligned **fuse** structure with increased d. and reduced thermal exposure and method of fabrication with heat sink)
Laser radiation
Nonvolatile memory devices
Photolithography
Semiconductor memory devices
(self-aligned **fuse** structure with increased d. and reduced thermal exposure and method of fabrication with heat sink)
IT **Polyimides**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(self-aligned **fuse** structure with increased d. and reduced thermal exposure and method of fabrication with heat sink)

L16 ANSWER 14 OF 20 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2000-255702 [22] WPIX Full-text
TI Fabrication of **fuse** on surface of **semiconductor** device circuitry which is coplanar with surrounding dielectric, comprises patterning layer of **fuse** material through photoresist mask and forming contacts through passivation layer.
IN AGARWALA, B N; DALAL, H M; NGUYEN, D B; RATHORE, H S
PA (IBMC) INT BUSINESS MACHINES CORP
PI US 6033939 A 20000307 (200022)* 7p H01L021-82
PRAI US 1998-63992 19980421
AB US 6033939 A UPAB: 20000508
NOVELTY - A **fuse** for a programmable **semiconductor** device is formed by depositing a thin layer of **fuse** material on a planarized surface of circuitry and insulation and patterning the layer through a photoresist mask. A passivation layer is then added and contact vias are formed to adjacent circuitry lines connected by the **fuse** .

DETAILED DESCRIPTION - The **fuse** is programmable by low voltage pulses or **laser** pulses. Contacts to the adjacent circuitry are formed by forming damascene via studs and adding metal pads on the surface.

USE - In fabrication of **semiconductor fuse** devices programmable by **laser** pulses or voltage pulses below about 3.5V.

ADVANTAGE - Reliable **fuse** links are fabricated in high yield.

DESCRIPTION OF DRAWING(S) - The drawing shows a **fuse** link device formed by the method of the invention with C4 solder bumps. Cu lines 1
Via studs 2
Semiconductor substrate 3
Passivation layer 4
Fuse layer 5
Oxide 6
Nitride 7
Polyimide 8
Terminal studs 9
Pads 10
C4 solder balls 11
Dwg.4/4

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - The **fuse** material is metallic, preferably Si-Cr oxide, Ta, TaN, Ti, TiN, W, W-Si, Si, Ge, SiC or GeC, and is deposited. . . . are used for wire bonding, TAB connection or C4 solder ball connection.

TECHNOLOGY FOCUS - POLYMERS - Preferred Method: The **fuse** material may alternatively be **organic**, preferably **polyaniline**.

L16 ANSWER 12 OF 20 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2001-137243 [14] WPIX Full-text
TI Formation of **laser** accessible **fuse** for memory arrays by forming **fuse** with rupture zone, patterning metal layer to form conductive wiring connected to conductive contacts, plate over rupture zone, and wiring pad, patterning passivation layer.
IN LIN, H; TZENG, W; YANG, C
PA (VANG-N) VANGUARD INT SEMICONDUCTOR CORP
PI US 6180503 B1 20010130 (200114)* 17p H01L021-44
PRAI US 1999-354852 19990729
AB US 6180503 B UPAB: 20010312
NOVELTY - A **laser** accessible **fuse** is formed by forming a **fuse** with a rupture zone; patterning a metal layer to form conductive wiring connected to at least two conductive contacts, a plate over the rupture zone, and a wiring pad; patterning a passivation layer by anisotropically etching the passivation layer and an anti-reflective coating over a bonding pad, forming a **laser** access window.

DETAILED DESCRIPTION - A **laser** accessible **fuse** is formed by:

(a) depositing a layer of **fusible** material on a first insulative layer on a silicon wafer (70);

(b) patterning the layer of **fusible** material to form a **fuse** (78) with a rupture zone (78A);

(c) depositing a second insulative layer over the wafer;

(d) forming conductive contacts to the **fuse** through openings in the second insulative layer, where the rupture zone is connected between, and in electrical series with, at least two of the conductive contacts;

(e) depositing a first metal layer (94) on the second insulative layer;

(f) patterning the first metal layer to form conductive wiring (96) connected to each of at least two conductive contacts, a plate (86) over the rupture zone, and a wiring pad;

(g) depositing a third insulative layer over the wafer;

(h) patterning the third insulative layer to form a via opening to the wiring pad, and a window opening over the rupture zone;

(i) depositing a second metal layer (108) on the wafer;

(j) depositing an anti-reflective coating (92) on the second metal layer;

(k) patterning a bonding pad in the second metal layer over the via opening and removing the anti-reflective coating, the second metal layer, and the first metal layer in the window opening;

(l) depositing a passivation layer over the wafer; and

(m) patterning the passivation layer by anisotropically etching the passivation layer and the anti-reflective coating over the bonding pad while simultaneously etching a region within the window opening, penetrating the second insulative layer to a final second insulative layer thickness over the rupture zone, forming a **laser** access window.

TECH UPTX: 20010312
TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The **fusible** material is polysilicon. The first metal layer comprises aluminum, tungsten, copper, or their alloys. The anti-reflective coating comprises titanium nitride, . . . silicon oxide (118), an intermediate layer of silicon nitride (119) (superjacent to the bottom layer), and a top layer of **polyimide** (120).
Preferred Property: The second and the third insulative layers are 0.8-1.3 microns thick. The laminar structure of the passivation layer. . .

L16 ANSWER 11 OF 20 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2001-535463 [59] WPIX Full-text
TI **Semiconductor fuse** structure formation method, involves filling hole formed on dielectric layer with conductive **fuse** material for electrical connection between conductive lines formed on dielectric material.
IN DAUBENSPECK, T H; MOTSIFF, W T; RANKIN, J H
PA (IBMC) INT BUSINESS MACHINES CORP
PI US 2001014509 A1 20010816 (200159)* 11p H01L021-20
US 6440834 B2 20020827 (200259) H01L021-44
PRAI US 1999-326437 19990604; US 2001-827871 20010406
AB US2001014509 A UPAB: 20020919
NOVELTY - Conductive lines are formed in dielectric layer (A) (18) which is formed on surface of semiconductor structure. Dielectric layer (B) (22) is formed over layer (A) such that conductive lines are covered. A hole is formed on layer (B) to expose a portion of conductive lines, and hole is filled with conductive **fuse** material (26) so that an electrical connection is provided between conductive lines.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The substrate is a semiconducting material chosen from silicon, germanium, silicon germanide, gallium arsenide, indium arsenide, indium phosphide, other III/V compounds and **organic** semiconductors. The conductive region comprises noble metal, noble metal oxide, conductive oxide or their mixtures. The dielectric layers (A and B) comprises same or different dielectric material chosen from silica, silicon nitride, **diamond** , **diamond**-like **carbon** and porous glass.

TECHNOLOGY FOCUS - POLYMERS - Preferred Materials: The dielectric layers (A and B) comprises same or different dielectric material chosen from paralyene polymers, **polyimides** and silicon-containing **polymers**. The **conductive fuse** material comprises doped **conductive polymer** comprising **polyaniline**, polypyrrole or polyalkylthiophene.

L16 ANSWER 9 OF 20 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2002-266393 [31] WPIX Full-text
TI **Fuse** blowing process in **semiconductor** chips, involves etching **fuse** link after removing insulator formed above **fuse** link.
IN MOTSIFF, W T; PREVITI-KELLY, R A; PRICER, W D
PA (IBMC) INT BUSINESS MACHINES CORP
PI US 6335229 B1 20020101 (200231)* 11p H01L021-82
PRAI US 1999-417289 19991013
AB US 6335229 B UPAB: 20031112
NOVELTY - An insulator formed above the **fuse** link, is removed by ablating the insulator using **laser** or **ultraviolet light** whose energy level is below the level that has an effect on the **fuse** link.

The **fuse** link is then etched by either dry or wet etching.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for inductive device programming method.

USE - For blowing up **fuse** in **semiconductor** chips to provide redundancy, electrical chip identification and customization of function.

ADVANTAGE - The fragile low K dielectric such as **polyimide** nanofoam, is not exposed to the high internal pressures and high local temperatures, thus blowing the **fuse** does not damage the surrounding dielectric material. The link that is opened is physically isolated from the remainder of the wiring and circuitry on the integrated circuit device and hence isolation and lack of DC bias across the opened **fuse**, corrosion of the active link after **fuse** blow has no impact on the state of the blown **fuse** and other wiring structures in the device.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic top and side views of inductive **fuse**.

Dwg.3, 4/20

L16 ANSWER 8 OF 20 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2002-689385 [74] WPIX Full-text
TI **Semiconductor** device **fuse** production comprises forming dielectric layer with first region overlying **fuse** material to be blown, and depositing and patterning photoresist mask to exposed second region of the dielectric layer.
IN CASTAGNETTI, R; GIUST, G K; LIU, Y; RAMESH, S
PA (LSIL-N) LSI LOGIC CORP
PI US 6413848 B1 20020702 (200274)* 11p H01L021-44
PRAI US 1998-118231 19980717; US 2000-534907 20000323
AB US 6413848 B UPAB: 20021118
NOVELTY - Production of a **semiconductor** device **fuse** comprises forming a dielectric material layer having a first region overlying a portion of a **fuse** material to be blown and a second region bounding the first region. A photoresist mask is deposited and patterned to exposed the second region of the dielectric material, which is removed to reduce the thickness of the dielectric in the patterned region.

DETAILED DESCRIPTION - The production of a **semiconductor** device **fuse** involves forming a dielectric material layer on a portion of a **fuse** material. The dielectric material layer has a first region overlying a portion of the **fuse** material to be blown and a second region bounding the first region. A photoresist mask is deposited and pattern on a portion of the dielectric material so that the second region of the dielectric material is exposed. A portion of the dielectric material is removed in the exposed patterned region to reduce the thickness of the dielectric in the patterned region. The photoresist mask is then removed after the removal of the dielectric material portion. The reflectance of incident **laser light** from the dielectric in the first region is less than that from the dielectric in the second region.

USE - For the production of a **semiconductor** device **fuse**.

TECHNOLOGY FOCUS - POLYMERS - Preferred Material: The dielectric may comprise **polyimide**.

L16 ANSWER 7 OF 20 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2003-015727 [01] WPIX Full-text
TI Self-passivating copper-**laser fuse** for **semiconductor** devices, has passivation areas on open **fuse** surface and in specified interfaces that are subjected to **laser** energizing.
IN BARTH, H; BARTH, H J
PA (BART-I) BARTH H; (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP
PI US 2002084507 A1 20020704 (200301)* 5p H01L021-82
PRAI US 2000-751554 20001228
AB US2002084507 A UPAB: 20030101
NOVELTY - A self-passivating copper-**laser fuse** includes passivation areas on the open copper-**fuse** surface; and in the interfaces between the copper-alloy seed layer and the liners and dielectric, and between the pure copper layer and the dielectric cap, that are subjected to energizing **laser**.

DETAILED DESCRIPTION - A self-passivating copper (Cu) (16)- **laser fuse** comprises a metallization-line (13); a liner separating the metallization line and a combination Cu-alloy seed layer and pure Cu layer, a dielectric (14) surrounding the liner; and a dielectric cap disposed over the surrounding dielectric, the liner and the combination Cu-alloy seed layer and pure Cu layer. The passivation areas on the open Cu-**fuse** surface; and in the interfaces between the Cu-alloy seed layer and the liners and dielectric, and between the pure Cu layer and the dielectric cap, are subjected to energizing **laser**. An INDEPENDENT CLAIM is also included for a process of preparing an integrated circuit structure comprising:

(a) patterning a Damascene structure in a dielectric to form a **fuse**;
(b) depositing a metallic liner;
(c) depositing a seed-layer of a Cu-alloy for a Cu-fill;
(d) filling the Damascene structure with a pure Cu;
(e) pre-CMP annealing at low temperatures less than 200 deg. C;
(f) CMP Cu to remove Cu-overfill followed by CMP liner;
(g) depositing a dielectric cap layer;
(h) depositing final passivation layer;
(i) thinning dielectric layer or final passivation layer on top of the **laser fuse**;
(j) **laser** fusing the metal **fuse** to form crater in the surrounding area of the blown Cu **fuse**;
(k) annealing the **fuse** at 250 - 450 deg. C to form a Cu **laser** characterized self-passivating areas.

USE - For semiconductor devices.

ADVANTAGE - The self-passivating Cu-**laser fuse** of the invention has resistance to oxidation and corrosion and improved adhesion in the interface between Cu and metallization lines and Cu and a dielectric cap subsequent to blowing the **fuse** by an energizing **laser**.

TECHNOLOGY FOCUS - POLYMERS - Preferred Method: Between steps (h) and (i) deposition of a **polyimide** or **photo**-sensitive **polyimide** is performed.

L16 ANSWER 3 OF 20 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2003-851484 [79] WPIX Full-text
TI **Fusible** link for **semiconductor** device, has insulating substrate, conductive line pair, and polymer capable of being changed from non-conductive to conductive state upon exposure to energy beam.
IN DAUBENSPECK, T H; KLAASEN, W A; MOTSIFF, W T; PREVITI-KELLY, R A; RANKIN, J H
PA (IBMC) INT BUSINESS MACHINES CORP
PI US 2002182837 A1 20021205 (200379)* 10p H01L021-44
PRAI US 1999-417853 19991014; US 2002-159573 20020531
AB US2002182837 A UPAB: 20031208
NOVELTY - A **fusible** link comprises an insulating substrate; a conductive line pair on the surface of the insulating substrate, and having spaced ends; and a polymer over the insulating substrate and between the line pair ends. The polymer is capable of being changed from a non-conductive to a conductive state upon exposure to an energy beam.

(b) a method of making a **fuse** for a **semiconductor** device, comprising providing an insulating substrate (20) having a surface; forming a conductive line pair on the substrate surface; forming over the insulating substrate and between the line pair ends a polymer layer (30) capable of carbonizing when exposed to an ion or other energy beam for a time to become electrically conductive; and

USE - For a semiconductor device, e.g. an integrated circuit device (e.g., a semiconductor chip to provide redundancy, electrical chip identification and customization of function).

ADVANTAGE - The invention avoids the need to physically blow **fuses** by utilizing polymers that can be made to become conductive upon exposure to a **laser** or other energy source. The structure allows formation of **fuses** with either polymer or glass low dielectric constant films with minimum impact to the dielectric structure. The invention provides a **fuse** structure that is compatible with nanopore/nanofoam low dielectric constant insulating films required for advanced **integrated circuit** devices. It provides a **fuse** structure (or antifuse) in which desired circuits are initially left open in a **fuse** area (40). The **fuse** area may left non-conductive or be made conductive, if desired, by exposure to the energy beam to program the integrated circuit device in the desired manner. The invention overcomes the limitations of prior art **fuse** structures and methods of making the **fuse**, and avoids the need to physically blow **fuses**. It also avoids the problem of exposed copper after **fuse** blow, and allows the use of composite final metals that are otherwise difficult to use as **laser fusible** links. It allows exotic composite conductors to be used at final metal, because **fuse** blow is no longer a consideration. It also solves the problem of fusing for semiconductor chips when low k **organic** foams and glasses are used for interlevel dielectrics.

TECHNOLOGY FOCUS - POLYMERS - Preferred Component: The polymer comprises a **polyimide** capable of carbonizing when exposed to an ion or other energy beam for a time to become electrically **conductive**; a photoconductive **polymer** material, preferably a polymer/onium salt mixture; or a **polyaniline** polymer doped with a triphenylsulfonium salt.

L30 ANSWER 2 OF 24 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:211054 HCAPLUS Full-text
TI Semiconductor integrated circuit device and its production method.
IN Tsura, Katsuhiko
PA Matsushita Electronics Corp., Japan

PI	JP 2001077202	A2	20010323	JP 2000-38511	20000216
	US 6562674	B1	20030513	US 2000-599354	20000621
	US 2003146491	A1	20030807	US 2003-369548	20030221 <--
	US 6677195	B2	20040113		
PRAI	JP 1999-191798	A	19990706		
	US 2000-599354	A3	20000621 <--		

AB [Machine Translation of Descriptors]. Minuteness * corresponding to high integration, shortening the formation time of the opening of top of the fuse without causing the decrease of the reliability with the cutting of the **fuse** section in the **semiconductor integrated circuit** device which multilayer interconnection is converted, and the decrease of production yield rate, section, shortens production time. On insulator film 12 between the layer, fuse section 13 and padding electrode 17 the formation it does with the metal wiring layer of the most upper layer, inorganic insulated protective **coat** 14 the formation does the opening 18 after the formation and top of padding electrode 17 on that. Extensively to apply the **organic** insulated protective **coat** 15 of the photosensitive, pattern j0 doing, on top of fuse section 13 opening the formation it does opening 19 on top of 16 and padding electrode 17. Etching inorganic insulated protective **coat** 14 according to need, it makes the film thickness of inorganic insulated protective **coat** 14 of top of fuse section 13 thin.

IC ICM H01L021-82
ICS H01L021-3205

L30 ANSWER 3 OF 24 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:73502 HCAPLUS
TI Passivation layer etching process for memory arrays with fusible links
IN Tzeng, Wen-Tsing; Yang, Chun-Pin; Lin, Hsing-Lien
PA Vanguard International Semiconductor Corporation, Taiwan
PI US 6180503 B1 20010130 US 1999-354852 19990729 <--
PRAI US 1999-354852 19990729 <--
AB A method is described for progressively forming a **fuse** access openings in **integrated circuits** which are built with redundancy and use laser trimming to remove and insert circuit sections. The fuses are formed in a polysilicon layer and covered by ≥1 relatively thin insulative layers. An etch stop is patterned over the fuse in a higher level polysilicon layer or a 1st metalization layer. Addnl. insulative layers such as inter-metal dielec. layers are then formed over the etch stop. A 1st portion of the laser access window is then etched during the via etch for the top metalization level. The etch stop prevents removal of the insulation subjacent to it. Cumulative thickness non-uniformities in the relatively thick upper insulative layers are thus removed from the fuse window. The etch stop is removed during patterning of the top level metalization. A passivation layer is applied and patterned to exposed bonding pads and, at the same time complete the etching of the laser access window to a desired thickness over the fuses. The passivation layer over etch required to penetrate the insulation layer over the fuses also removes an antireflective **coating** over the bonding pads. The process fit conveniently within the framework of an existing process and does not introduce any addnl. steps. In addition, the passivation layer can be patterned to form final access to both bonding pads and laser access openings with a single photolithog. mask.
IC ICM H01L021-44
ICS H01L021-332
IT **Polyimides**, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(device passivation layer; passivation layer etching process for memory arrays with fusible links)
IT 11105-01-4, Silicon nitride oxide 12033-62-4, **Tantalum nitride (TaN)** 25583-20-4, **Titanium nitride (TiN)**
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(antireflective **coating**; passivation layer etching process for memory arrays with fusible links)

L30 ANSWER 4 OF 24 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:155186 HCAPLUS
TI Method for providing electrically fusible links in copper interconnection
IN Agarwala, Birendra N.; Dalal, Hormazdyar M.; Nguyen, Du B.; Rathore, Hazara S.
PA International Business Machines Corporation, USA
PI US 6033939 A 20000307 US 1998-63992 19980421 <--
PRAI US 1998-63992 19980421 <--
AB A method is provided for the fabrication of **fuses** within a **semiconductor IC** structure, which **fuses** are deletable by a laser pulse or a low-voltage elec. pulse typically below 3.5 V to reroute the elec. circuitry of the structure to remove a faulty element. The fuses are formed on the surface of circuitry which is coplanar with a surrounding dielec. such as the circuitry formed by a damascene method. A preferred fuse material is Si-Cr-O and the preferred circuitry is Cu.
IC ICM H01L021-82
NCL 438132000
IT **Polyanilines** — used for fuse link
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(providing elec. **fusible links** in copper interconnections for **integrated circuits** containing)
IT 409-21-2, Silicon carbide (SiC), processes 7440-21-3, Silicon, processes 7440-25-7, Tantalum, processes 7440-32-6, Titanium, processes 7440-33-7, Tungsten, processes 7440-56-4, Germanium, processes 12033-62-4, Tantalum nitride (TaN) 25583-20-4, Titanium nitride (TiN) 51637-10-6 67527-63-3, Germanium carbide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(providing elec. **fusible links** in copper interconnections for **integrated circuits** containing)

L30 ANSWER 5 OF 24 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:557245 HCAPLUS
TI Semiconductor memory devices, fabrication, and protective sheets for fabrication thereof
IN Yamashita, Masayuki; Kawamura, Hideki; Akai, Kiyoyasu
PA Mitsubishi Electric Corp., Japan
PI JP 11238856 A2 19990831 JP 1998-40252 19980223
PRAI JP 1998-40252 19980223
AB An elongated fuse is formed on an insulated substrate, covered on its top by a protective film, and is partly exposed out of an opening of the protecting film so that the exposed portion of the fuse is cut to disconnect upon replacement of damaged memory cells by stand-by extra memory cells. The protective film is cut out of a large protective sheet laminated on a base tape. The protective film is removed after polishing the substrate to protect the remaining polymer layer.
IC ICM H01L027-10
ICS H01L021-304; H01L021-82
IT Electric **fuses**
(for replacement of memory cells; **semiconductor** memory devices and fabrication and protective sheets for fabrication thereof)
IT **Coating** materials
(polymer; semiconductor memory devices and fabrication and protective sheets for fabrication thereof)
IT **Polyimides**, properties
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PRP (Properties); PROC (Process); USES (Uses)
(protective film; semiconductor memory devices and fabrication and protective sheets for fabrication thereof)

L30 ANSWER 6 OF 24 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1994:180635 HCAPLUS
TI Manufacture of semiconductor device
IN Watanabe, Kunio
PA Nippon Electric Co, Japan
PI JP 05251564 A2 19930928 JP 1992-38929 19920226
PRAI JP 1992-38929 19920226
AB The title process comprises formation of a passivation film on a device having bonding pads and fuse elements (e.g., for redundant circuits of a memory device) and patterning thereof to form openings on the bonding pads and the fuse elements, necessary cut of fuse elements by a laser beam based on preliminary testing of elec. characteristics, application of an α-ray shielding resin (e.g., **polyimide**) on the surface and patterning thereof to form openings on the bonding pads, and heat treatment and elec. testing of the device. Moisture resistance of the uncut fuse elements is kept by the resin film.
IC ICM H01L021-82
ICS H01L021-66; H01L023-02; H01L023-29; H01L023-31; H01L027-10
IT **Polyimides**, uses
RL: USES (Uses)
(**coating** of **semiconductor** devices with, after cutting of **fuse** elements)
IT **Coating** materials
(**polyimide**, on **semiconductor** devices with **fuse** elements cut)
IT **Semiconductor** devices
(post-testing cutting of **fuse** elements and surface resin **coating** in manufacture of)

L30 ANSWER 7 OF 24 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1986:601578 HCAPLUS
TI A **semiconductor** device with improved **fuse** melting by laser radiation
IN Saito, Shozo
PA Toshiba Corp., Japan
PI US 4602420 A 19860729 US 1984-681294 19841213
JP 05019817 B4 19930317 JP 1984-32830 19840223
PRAI JP 1984-32830 19840223
AB In manufacturing a semiconductor device, the device architecture allows improved melting of fuse elements by laser radiation.
IC ICM H01L021-263
ICS B23K026-00
IT **Polyimides**, uses and miscellaneous
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(alpha-particle screening layers from, in semiconductor devices)
IT **Semiconductor** devices
(**fuse** melting by laser radiation for)

L30 ANSWER 9 OF 24 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2003-799854 [75] WPIX Full-text
TI Formation of passivation **coating** on semiconductor wafer, by patterning and etching first dielectric layer using first photomask, patterning third dielectric layer using second photomask, and etching second dielectric using **polyimide** pattern.
IN HSU, Y
PA (HSUY-I) HSU Y
PI US 6589712 B1 20030708 (200375)* 12p G03C005-00
PRAI **US 1998-186262 19981104**
AB US 6589712 B UPAB: 20031120
NOVELTY - Formation of passivation **coating** on semiconductor wafer, by patterning and etching first dielectric layer using first photomask, patterning third dielectric layer using second photomask, and etching second dielectric using **polyimide** pattern.

DETAILED DESCRIPTION - Formation of a passivation **coating** on a semiconductor wafer involves forming a first dielectric layer on the wafer comprising a first area having a **fuse**, a **semiconductor** device, and an oxide layer (33) with a fuse window; and a second area having a bonding pad with a metal layer (43). The fuse is at the bottom of the fuse window. The first dielectric layer is patterned and etched to expose the fuse window and metal layer according to a first photomask. A second dielectric layer is formed on the first dielectric layer, fuse window, and metal layer. A third dielectric layer made of **polyimide** is formed on the second dielectric layer. It is patterned by exposing the third layer through a second photomask using a photolithographic tool to form a **polyimide** pattern exposing a portion of the second dielectric layer. The **polyimide** is a negative photoresist (45) having a thickness of 5 mu m. The exposed portion of the second dielectric layer is etched to form a spacer on the sidewall of the fuse (37) and fuse window (35) and to expose the metal layer. The second dielectric layer is etched by an anisotropic etching using the **polyimide** pattern as a mask. The passivation **coating** on the wafer is fabricated by etching the three dielectric layers according to the photomasks.

L30 ANSWER 10 OF 24 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2002-253492 [30] WPIX Full-text
TI Laser accessible **fuse** formation in **integrated circuit** comprises etching laser access opening in two steps using transient etch stop layers to limit access opening depth after first step and finishing opening in second step.
IN CHEN, Y; TZENG, W; WANG, K
PA (VANG-N) VANGUARD INT SEMICONDUCTOR CORP
PI US 6294474 B1 20010925 (200230)* 11p H01L021-302
PRAI **US 1999-425906 19991025**
AB US 6294474 B UPAB: 20020513
NOVELTY - A laser accessible **fuse** is formed in an **integrated circuit** by etching a laser access opening in two steps using a transient etch stop layers to limit the depth of the access opening after the first step and finishing the opening in the second step.

DETAILED DESCRIPTION - Formation of a laser accessible **fuse** in an **integrated circuit** involves:

(a) providing a silicon wafer (10) having integrated circuit devices and a first insulative layer;

(b) patterning a fusible material layer on the first insulative layer to form a fuse (18) with a rupture zone;

(c) depositing a silicon oxide layer on the wafer;

(d) patterning a polysilicon layer over the silicon oxide layer to form a first plate overlying the rupture zone;

(e) depositing a second insulative layer over the wafer;

(f) forming conductive contacts to the fuse on through openings in the second insulative layer and the silicon oxide layer, by which the rupture zone is connected between, and in electrical series with, at least two of the conductive contacts;

(g) patterning a first metal layer (34) having a super-adjacent first antireflective **coating** (ARC), on the second insulative layer to form a first inter-connective wiring level to the devices and the fuse, and a second plate, concentric with the first plate overlying the rupture zone;

(h) depositing a third insulative layer over the wafer;

(i) patterning the third insulative layer and penetrating first ARC, to form via openings and an access opening (46) which exposes the second plate;

(j) patterning a second metal layer (50) having a super-adjacent second ARC, on the third insulative layer to form bonding pads connected to the inter-connective wiring through vias in the third insulative layer, while simultaneously removing both the second metal layer and the second plate in the access opening;

(k) depositing a passivation layer (68) on the wafer;

(l) patterning the passivation layer and the ARC by anisotropically etching, with a first etchant gas mixture and a first silicon oxide-to-polysilicon selectivity, to expose the bonding pads and a region within the window opening, penetrating the third and second insulative layers, and stopping on the first plate; and

(m) after step (l), without breaking vacuum and with a second gas mixture and a second silicon oxide-to-polysilicon selectivity, etching through the first plate and partially into the second insulative layer, leaving a final thickness of the second insulative layer over the rupture zone.

L30 ANSWER 13 OF 24 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 2001-185600 [19] WPIX Full-text
TI Semiconductor device e.g. large capacity semiconductor memory, LSI system, has p-SiN formed on p-TEOS film, by which plasma etching is performed via openings.
PA (MATE) MATSUSHITA ELECTRONICS CORP
PI JP 2000357743 A 20001226 (200119)* 7p H01L021-82
PRAI JP 1999-169145 19990616
AB JP2000357743 A UPAB: 20010405
NOVELTY - A p-TEOS film (13) is formed on a redundant fuse (11) and a bonding pad (12) which are covered by a protective **coat**. A p-SiN film (14) by which plasma etching is performed via openings (16,17) is formed on p-TEOS film. A **polyimide** film (18) is formed on the p-SiN film.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for semiconductor device manufacturing method.

USE - Semiconductor device e.g. large capacity semiconductor memory, LSI system used for digitization of electronic device.

ADVANTAGE - The film thickness of p-TEOS film on redundant **fuse** is controlled correctly, hence reliable **semiconductor** device is materialized by using comparatively inexpensive plasma etching apparatus.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view showing the manufacturing method of semiconductor device.

Redundant fuse 11
Bonding pad 12
p-TEOS film 13
p-SiN film 14
Openings 16,17
Polyimide film 18

L30 ANSWER 20 OF 24 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN 1984-197355 [32] WPIX Full-text
TI Resistor used as **fuse** in **semiconductor IC** - is produced by selectively implanting argon ions into **polyimide** resin film **coated** on semiconductor substrate NoAbstract Dwg 3,4/5.
PA (TOKE) TOKYO SHIBAURA DENKI KK
PI JP 59111353 A 19840627 (198432)* 10p
PRAI JP 1982-221325 19821217
TI Resistor used as **fuse** in **semiconductor IC** - is produced by selectively implanting argon ions into **polyimide** resin film **coated** on semiconductor substrate NoAbstract Dwg 3,4/5.